Expertise in VLSI (Very Large Scale Integration) and EDA (Engineering Design Automation):

I have been active in these areas since 1985. I have co-authored with Dr. Ed Fernandez, a book, VLSI and Computer Architecture, published by Academic Press Inc. in 1989. He has been a consultant to IBM, Aptek, and Motorola, since 1985. I also worked as an R&D engineer with the computer division of the Electronic Corporation of India Ltd. (HCIL), Hyderabad, India, immediately after my graduation with a BS. In 1993, Motorola recognized the relevance of my efforts in EDA and helped me establish the Center for VLSI and Systems Integration (CVSI) with generous grants, EDA Vendor tools, NSF matching funds, and access to Motorola resources. Many Motorola engineers have continued to help on their own. Motorola has two major divisions in Boynton Beach (now part of Freescale) and Plantation, FL, within about 30 miles distance from the main campus of the university. The highlights of this interaction were covered in the 1996 annual newsletter of the College of Engineering. Focus at CVSI is on portable communication systems. My related research expertise is in mixed mode system design, structured design, and EDA tool integration. More recently, since 2003, I have focused on system integration issues, a natural culmination of this varied background. I have undergone training of many EDA tool vendors, such as Cadence, Synopsys, Mentor Graphics, Silvaco, Analogy, Cascade, Hewlett Packard, Xilinx, Daizix, and others, on tools at various levels of system and IC design, simulation and testing. All my courses at the university have a strong component of hands-on design experience with commercial EDA tools.

I taught courses on VLSI during 1986-1999 on: Introduction to VLSI, Structured VLSI Deisgn, Advanced Topics in VLSI Design (Low Power Design, SOI), VLSI and Computer Architecture, Analog and Neural VLSI, and Microelectromechanical Systems (with Dr. Masory, ME). I taught courses on Engineering Design Automation during 1985-2000 on: CAD-Based Computer Design, with Verilog; Structured Digital Design; Computer Hardware Design I and II; Semi-Custom VLSI Design with DSP (With Dr. Sudhakar, EE). I have guided 14 MS theses and 2 Ph.D. disserations in these areas since 1990. Seven Chips were designed and fabricated at MOSIS during 1990s, as pertinent to research and theses projects, on: Op Amp Building Blocks; Artificial Neural Network ; Signature Analyzer; Analog Cell Library for Neural Nets; RISC II Register File; Parallel Distributed Thinning, and Bit Serial DSP Building Blocks. The goal has always been to develop regular architectures and scalable building blocks. I have received one US patent in this area, on a highly scalable multiplier, and has one regular patent and 2 provisional patents filed that expand on this concept. I have received $ 1.6 Million in federal and industrial grants in the areas of VLSI and Deisgn Automation. More recently (2003-2007), I have received $1.035 Million (as PI, with Drs. Furht and Agarwal as Co-PIs) grants from Motorola on the OPP Project, a systems integration project, described in more detail under the Systems Integration category.