Characterized Analog Cell Library For Artificial Neural Networks

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I. ABSTRACT

Traditional digital computers are not good at cognitive tasks, such as vision, speech, and motor control, which are easy for the mammalian nervous system. Artificial Neural Networks (ANN) have evolved in an attempt to emulate the parallel distributed processing of the brain. We have evolved a comprehensive low power dissipation, high density analog ANN cell (or building block) library that is compatible with a standard digital VLSI technology. Considerable interest exists in industry and academia for such a cell library and support environment. The cell library was recently donated to the MOSIS Users Group (MUG).

II. INTRODUCTION

Artificial Neural Networks (ANN) have been evolved in an attempt to emulate the parallel distributed processing of the brain. Parallel distributed processing models are useful for cognitive tasks that require massive constraint satisfaction, i.e., the parallel evaluation of many clues and facts and their interpretation in the light of numerous interrelated constraints. Cognitive tasks such as vision, speech, language processing, and motor control, are also characterized by a high degree of uncertainty and variability and traditional Von Neumann computers do not provide good performance.

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In general, an Artificial Neural Network (ANN) is a massively parallel information processing architecture composed of many simple processing elements interconnected to achieve collective computational capabilities [1, 2, 3]. The feature that most distinguishes neural network processing from conventional signal processing is the ability to internally develop, or "learn" the algorithms required for process detection and classification [4]. In addition, the neural networks are re-trainable for whole new classes of particular signal processing problems. The first neural network applications were built and successfully demonstrated over thirty years ago. Neurocomputing has seen a resurgence of interest due to the maturation of silicon VLSI circuit technology. The application of artificial neural network technology promises advantages in speed, fault tolerance, and development effort over conventional approaches. Implementation of real-time algorithms with neural networks is feasible.

Professor Carver Mead at California Institute of Technology has evolved innovative neural networks using VLSI technology [5]. His effort is directed to the development of circuitry modeled as closely as possible on the structure of mammalian sensory systems. Mead's view of neural networks considers the problem of neural network fabrication as a branch of analog circuit design.

Impressive results have been achieved to date, with the development of models of the mammalian cochlea and retina. As a result of these models, and the supporting development of CMOS circuitry which operates in the subthreshold region, complex VLSI realizations have been reported [5, 6, 7]. Successful application of the subthreshold Operational Transconductance Amplifier (OTA) to these models suggests further research into the application of the technology in the development of a neural network cells, and more conventional subthreshold analog signal processing circuits. We have implemented a library of such cells [8, 9].

Our present implementations are possible only in a single technology and set of scale rules [8, 9]. We expect to further improve them to be scaleable and independent of the implementation technology. The library will continue to be compatible with a standard digital CMOS technology

for mixed analog/digital designs. In addition, we shall to continue develop an even more comprehensive cell library and determine the limits of scaleability.

Today, the only practical ANN information processing hardware implementations are in VLSI technologies. The immense cost incurred in developing a hardware technology to the point of usefulness for practical applications implies the need for creating a public "VLSI ANN hardware cell library." With such a characterized library the experimenter can simulate the hardware using the building blocks from the library, test the design, and then fabricate the physical hardware. This approach will dramatically shorten the design cycle and reduce the cost of the completed design. Considerable interest exists in industry and academia for such a cell library.

The cells are realized as CMOS subthreshold analog circuits compatible with the fabrication services offered by the MOSIS fabrication service for application as: neural system building blocks, analog signal conditioning and filtering elements and blocks, and adaptive analog control elements and blocks. Analog signal processing circuits allow study of the acquisition and adaptation of filter weights by different algorithms, simultaneously providing the useful functions of adaptive filtering, adaptive equalization, and adaptive control.

One of the most obvious applications of trainable networks is to real-time signal processing problems. Nearly all conventional signal processing techniques employ special-purpose feature extraction hardware as an interface between the sensors and the detection/classification mechanism. Given requirements for minimum size, weight and power, a considerable advantage would be gained if this interface were simplified or eliminated [10, 11]. Further, decentralized control schemes, as evidenced with ANNs, are robust with respect to a wide range of parametric and non-linear time-varying uncertainties in their interconnection structure as well as subsystem dynamics [12].

III. THE CELL LIBRARY

The cell library circuits depend on subthreshold variations of the well understood operational transconductance amplifier (OTA) [13]. In the OTA, the output current is determined by the product of the input voltage difference and the transconductance as controlled by the bias input. The subthreshold [14] CMOS analog circuitry employed allows microwatt power levels at speeds sufficient for audio signal processing.

Our initial efforts in developing an analog cell library utilized a bulk CMOS 3 micron double poly single metal p-well technology supported by MOSIS, Univ. of South California, Marina del Rey, CA. We designed and laid out an amplifier, a resistor, a switch, a 12-bit capacitance array, current mirrors, and several digital cells needed to implement a Hamming type ANN.

Based on the above experience, we have now started developing a more comprehensive ANN cell library [8, 9] that is based on scaleable CMOS 2 micron double poly double metal p-well technology that MOSIS is supporting. We have designed the following circuits: A Transconductance Amplifier, A Wide-range Transconductance Amplifier, A Follower-integrator Circuit, A Wide-range Gilbert Multiplier, and A Current Mirror. These were designed based on the ideas of Mead [5], however the circuits shown had to be significantly modified to meet the specifications. We used the MAGIC graphics layout editor written at the University of California, Berkeley. The circuit simulations were analyzed using the HSPICE circuit analysis program written by Meta-Software, Inc. of Campbell, CA. Simulations were initially performed with SPICE parameters for a different MOSIS fabrication run and were repeated with the SPICE parameters obtained with the fabricated chips. The latter results are presented here.

Current Mirror

The simple N channel MOS current mirror, shown in Figure 1, is known as the Wilson current mirror. For equal sized devices, the circuit has a current gain of: $A_i = (1 + \lambda v_{D1}) / (1 + \lambda v_{D2}))$,

and the output impedance with no input current is: $R_{out} = (1 + \lambda v_{D2}) / (\lambda i_{D2}))$, where the channel length modulation factor λ depends on the device Early voltage.

The improved Wilson current mirror (as in Fig. 2) equalizes the drain potentials of devices Q_1 and Q_2 to make the current gain as precise as the ratio of the geometries of the devices and manufacturing tolerances allow. The output impedance is increased by the cascode action of the additional devices to: $R_{out} = (g_{m1} r_{ds1}) \cdot (g_{m3} / g_{m2}) \cdot r_{ds3}$, where g_m is the transconductance and r_{ds} is the incremental drain to source resistance.

The improved circuit may be used to achieve superior circuit performance, but does so at the cost of decreased dynamic output voltage range. The circuit cell size is not appreciably larger than the previous simple design, however, because the improved circuit may be constructed with minimum dimension devices while the simple circuit must use long channel devices to avoid the effects of the short channel Early voltage and to provide high output impedance. The current gain, A_i, depends on the W/L channel width to channel length) ratios of Q_1 and Q_2: $A_i = (W/L)_2 / (W/L)_1$ A similar circuit may be used for P channel devices and is shown in Fig. 3.

A modification of the Wilson current mirror is obtained by the addition of a resistor in the source lead of one of the devices Q_1 or Q_2 to make the current gain nonlinear. Addition of the resistor in the source lead of Q_1 shown in Fig. 2 provides the circuit shown in Fig. 4 known as an improved Widlar current mirror. The output impedance is increased by the cascode action of the additional devices similar to the improved Wilson design.

A useful advantage of the modification occurs because the gate voltages are equal, but the gate to source voltage may be very different. Large differences in device currents may be achieved with devices that are substantially the same size. For equally sized devices in Fig. 4, the output current will always be larger than the input. For output currents smaller than the input with equally sized devices, the resistor is placed in the source lead of the other grounded device. A similar circuit may be used for P channel devices and is shown in Fig. 5.

The wide range of current gains achievable using the Widlar current mirror with equally sized devices can often be used to advantage to provide a smaller area solution to a current mirror with large or small current gain than a Wilson current mirror. For the Widlar current mirror with unequally sized devices, the output currents may be smaller than the input over the low current part of the dynamic range, and yet larger than the input at higher outputs. Likewise, the nonlinearity may be used to provide output currents that are larger than the input at small currents and output that is smaller than the input at high currents.

Having both options available, expansion and compression of current gain with current level, provides useful applications in analog systems. One example, a cell in our library is shown by the current mirror reference circuit shown in Fig. 6.

Current Reference

The current mirror reference circuit consists of the connection of a P-channel Wilson current mirror and the N-channel Widlar current mirror in a feedback loop. The current gain of the P-channel Wilson current mirror is constant over the dynamic range, but the current gain of the Widlar current mirror changes with the current level. Selection of geometries in each mirror allows the loop gain to be greater than unity for small currents and less than unity for large currents. The action of the feedback stabilizes the loop at the level of current at which the loop gain is identically unity. Since the output impedances of the improved mirror circuits is very high, the currents are essentially invariant with changes in voltage, and the current mirror reference circuit provides a current reference that is independent of supply voltage variations.

The HSPICE simulation and fabrication test results are shown in Fig. 7. The initial discontinuity in HSPICE simulations is an artifact due to initial condition setting. Notice also the slight step in Fig. 7 (b): the reason for that is not clear at present. From the results, we also found that I_p or I_n changes from 14 nA to 17.4 nA when power supply voltage changes from 3 V to 10 V with the

relative change of 10.7%. Hence the current mirror reference circuit provides a current reference that is fairly independent of supply voltage variations. The cell size is 82 μm X 53 μm.

Simple OTA

The schematic diagram of a simple OTA is shown in Fig. 8. The circuit consists of the differential amplifier (Q1, Q2 and Qb) and a single current mirror (Q3 and Q4). Qb is used as a current source. Saturated current I_b set by the gate voltage V_b is divided between Q1 and Q2. Saturated drain current is exponential in the gate and source voltage: $I_{sat} = I_0 e^{(KVg-Vs)}$, where K depends on the fabrication process. Since $I_b = I_1 + I_2$, we obtain:

$$I_1 = I_b[e^{KV1} / (e^{KV1}+e^{KV2})] \text{ , and } I_2 = I_b[e^{KV2} / (e^{KV1}+e^{KV2})]$$

A current mirror is used to reflect current I_1, so the output current I_{out} is :

$$I_{out} = I_1 - I_2 = I_b \tanh[K(V_1-V_2)/2].$$

When the difference V_1-V_2 is small,

$$I_{out} = K[I_b(V_1-V_2)] / 2 = g_m(V_1-V_2)$$

The output current is a function of the difference between two input voltages V_1 and V_2. The transconductance g_m is proportional to the bias current I_b. The circuit also can be viewed as a two-quadrant multiplier.

Fig. 9 represents HSPICE simulation and test results for I_{out} when V_1 changes from 1.8 V to 3.2 V, for V_b = 0.4 V, 0.6 V, 0.8 V and 1.0 V. V_2 and V_{out} were fixed at 2.5V (half of the difference of Vdd and Vss). Fig. 10 shows test results for V_{out} when V_2 is fixed at 2.5 V and V_1 is changed from 2.3 V to 2.7 V, for V_b values of 0.4 V, 0.6 V, 0.8 V and 1.0 V. The size of the cell is 72 μm X 47 μm.

Wide-Range OTA

The simple transconductance Amplifier will not generate output voltages down to V_b below the lowest input signal that we have applied to it. This often is a source of problem at the system level. Fig. 11 shows a circuit with two additional current mirrors which can be used to improve the

performance. Figs. 12 (a) and (b) are HSPICE simulation and test results for I_{out}. Fig. 12 shows that output voltage can swing from Vdd to ground. Figs. 13 (a) and (b) are corresponding results for V_{out}. The threshold voltage was 0.83 V, leading to the discrepancy between the plots for V_{out}. The size of the cell is 83 μm X 54 μm.

Follower-Integrator Circuit (Single Pole)

Fig. 14 is a Follower-integrator (Mead nomenclature) circuit, with a voltage dependent time-constant single-pole filter characteristic. The circuit consists of an OTA connected as a follower, with its output driving a capacitor. For small signals, the capacitor C, charges at a rate proportional to the output current of the follower:

$$C\frac{dV_{out}}{dt} = G(V_{in}-V_{out}), \text{ and so } \frac{V_{out}(t)}{V_{in}(t)} = \frac{1}{\tau s + 1} \quad \text{where: } \tau = \frac{C}{G}$$

The response of the follower-integrator circuit is temporal-smoothed version of the input. Fig. 15 shows HSPICE simulation and test results of the circuit for a 40 mV step change in input voltage with quiescent input voltage equal to Vdd/2. The significantly higher rise time seen in the test results is due to the pad and load capacitances. Different transconductances of the amplifier are obtained by different V_b values. The cell size is 86 μm X 102 μm.

Capacitor Implementation

The capacitances above consist of the interlayer capacitance between a layer of polysilicon 1 covered by polysilicon 2 in addition to the capacitance between polysilicon 2 and a covering metal 1 layer. The largest contribution to the total capacitance value is due to the two layers of polysilicon, but the innovation of an additional layer offers other advantages besides an increase in capacitance per unit area.

Since one side of each capacitance is at AC ground potential, the structure chosen places the AC ground potential on the bottom layer of polysilicon 1 and the top layer of metal 1. Each capacitance is thus enclosed in its own Faraday shield to prevent unwanted parasitic capacitive coupling to

other nearby circuits. Sufficient overlap of the enclosing layers is also included to prevent coupling due to fringe fields at the periphery of the capacitances. Any additional circuitry may use the area above the capacitances for connections in metal 2 without the hazard of parasitic coupling.

Each capacitor is split into two equal parts. One half of each capacitor obtains AC ground from the Vdd supply bus, while the other half obtains AC ground from the GND supply bus. Charging currents are split so that only half is supplied from the power bus pair: while one half is being charged from the power bus pair, the other half is being discharged locally through the output devices. Without the split capacitor arrangement, using only the GND bus as AC ground, the full charging current is taken from the power bus during capacitor charge but is locally discharged through an output device during discharge. Since current is required from the power bus both during charge and discharge the magnitude is halved, but the frequency is doubled. The net gain is the reduction of signals on the power distribution system that are coherent with the signals being processed. The split capacitor arrangement also provides some measure of additional bypass at outputs due to the connection of capacitor halves between the buses.

The fabrication of capacitors in this manner does not allow precise calculation of time constant, but the matching of capacitance values may be made to within one percent. Since the time constants are calculated in the follower-integrator as the ratio of the capacitance to the transconductance, and the transconductance is an imprecise but adjustable parameter, these circuits are not particularly suitable for applications without some form of adaptive control.

Circuits with Complex Poles

A second order section, as in Fig. 16, is constructed from two follower-integrator cells and an additional OTA that allows the realization of complex poles with control over both the frequency and Q parameters. The second order sections have been fabricated, but the simulations have not been accomplished, and the fabrication test results that would verify the implementation, also have not been accomplished.

The circuitry thus far developed allows electrical control of pole placement, useful for some adaptive analog signal processing, but does not provide for selective control of zero locations. All zeroes are constrained to be placed at zero or infinity [15]. Research is required for the development of OTA circuits for the selective control of zero locations.

Multiplier

We have developed a multiplier cell originally designed by Barry Gilbert in 1968 and proposed by Mead as a useful subthreshold circuit block. The Gilbert multiplier provides an output current that is the product of the transconductance gain with the voltage differences A and B. The circuitry is far more complicated than a simple OTA, but it provides true four quadrant multiplication.

The original Gilbert multiplier was implemented in bipolar transistor technology and depends on exponential relationship between current and controlling voltage [16, 17]. Subthreshold operation of the MOSFET , due to the relationship between current and voltage being dominated by channel diffusion currents rather than drift currents, provides the necessary relationship.

Fig. 17 is the Gilbert Multiplier Circuit. The currents controlled by the differential voltage between terminal pair V_1-V_2 act as a pair of current sources for two other differential pairs. Five current mirrors are used to isolate the differential pairs. The drain currents of the differential pairs are:

$$I_1 = I_b / 2[1+\tanh K(V_1-V_2)/2],\ I_2 = I_b / 2[1+\tanh K(V_1-V_2)/2]$$

$$I_{13} = I_1 / 2[1+\tanh K(V_3-V_4)/2],\ I_{14} = I_1 / 2[1-\tanh K(V_3-V_4)/2]$$

$$I_{23} = I_2 / 2[1+\tanh K(V_3-V_4)/2],\ \text{and}\ \ I_{24} = I_2 / 2[1-\tanh K(V_3-V_4)/2]$$

The positive contribution to the output current, I^+ and negative contribution to the output current, I^- can be obtained as:

$$I^+ = I_{13} + I_{24} = (I_1+I_2)/2 + \{(I_1-I_2)\tanh[K(V_3-V_4)/2]\}/2, \text{ and}$$

$$I^- = I_{14} + I_{23} = (I_1+I_2)/2 - \{(I_1-I_2)\tanh[K(V_3-V_4)/2]\}/2$$

So; $I_{out} = I^+ - I^- = (I_1 - I_2) \tanh[K(V_3-V_4) / 2] = I_b \tanh[K(V_1-V_2)/2] \tanh[K(V_3-V_4) / 2]$ and, if the input voltage differences are small ($< KT/q\kappa$), then: $I_{out} = [K^2 I_b (V_1-V_2)(V_3-V_4)] / 4$, i.e., the output current is proportional to the product of input voltage differences (V_1-V_2) and (V_3-V_4).

Input and output voltages span the whole range of V_{dd} to ground. Fig. 18 shows HSPICE simulation and test results for I_{out} when $V_b = 1.5$ V, $V_{out} = 2.5$ V, and V_3-V_4 is changed from -0.2 V to 0.2 V (V_4 equals 1.5 V). Curves represent the input voltage (V_2-V_1) values in the range of $\pm$ 0.2 V respectively. The cell size is 131 μm X 77 μm.

IV. DISCUSSION

Scaleability Limitations

Small Early voltages (Va) were predicted (see Fig. 19) for the very small devices in the circuits implemented, resulting in departure from the more ideal behavior predicted by the larger devices used by Mead. Since the technology supports scaling to even smaller channel length, the circuits employed by Mead are not altogether satisfactory.

The consequence of small Early voltage is relatively high device output admittance, which is detrimental both to the gain and the output impedance of the current source required for a transconductance model. Lengthening the channel of crucial devices alleviates the problems encountered, however, this makes the circuits dependent on the scaling. Folded cascode circuitry [14] that improves electrical behavior while decreasing overall size, and the application of a Gilbert current gain stage to the folded cascode for further wideband gain, is being investigated to keep the functions independent of scaling.

OTA Modifications

The present OTA implementations rely on long channel output devices to attain high output impedance. Inherently, the long channel devices are dependent on the scale factor used in the implementation. The output stages can be made to have higher output impedance by making each

device a cascode connection of two devices. Dynamic range is usually reduced approximately by the gate to source voltage required to maintain the second device in the pinchoff region. Subthreshold operation reduces this gate to source voltage, and minimizes dynamic range reduction.

SPICE modeling of alternate output stages is being conducted: first, to determine feasible geometries and electrical constraints for devices in the proposed topology, then the MAGIC layout is performed for devices of those geometries, and finally, the SPICE parameters extracted and the results compared to preliminary models. The MAGIC layout editor extraction generates the capacitances, resistances, and parasitics that depend on the particular layout.

The differential stage of the OTA is usually loaded by two low impedance current mirrors which signal steering to the output stage. Interspersal of a folded cascode stage maintains the low impedance environment, while providing a point for the application of the Gilbert current amplifier. While additional current gain is not crucial for the improvement of the design of the OTA, it provides a degree of freedom in the tradeoffs encountered in scaling the design.

The Gilbert current gain stage maintains the bandwidth of the amplifier, while providing additional current gain, so there is no degradation of performance in bandwidth incurred by its use. Further, no additional bias voltages are required, so simplicity is maintained. The risk is deemed low in application of the above modifications to the basic OTA.

Filter and Control Transfer Functions

The OTA first order stage provides a lowpass filter function with an electrically controllable pole frequency. Development of topologies with electrically controllable zero locations, as well as the electrically controllable pole location, can proceed without prior development of the improved OTA. Performance, however, depends on the sensitivity of the topology to the parameters of the OTA and the variability of those same parameters, so alternate topologies must be considered and evaluated for minimum total sensitivity.

The OTA second order stage provides both lowpass and bandpass filter functions. Well known topologies are available for the computation of the highpass filter function by arithmetically combining the unfiltered signal with lowpass and bandpass outputs. Additionally, arithmetic combinations allow the generation of zeros in both the right and left half planes, however, the control algorithms for those topologies using OTAs and the sensitivity of the result is unknown. Continuous time controllers may be generated by the fabrication of rational form transfer functions with poles and zeros placed in the complex plane

Multiplier Modeling

The Gilbert multiplier cell has previously been analyzed as a bipolar circuit [13], and the subthreshold CMOS analysis following Mead is also complete [5]. The remaining modeling required represents the inclusions of parasitic capacitances and wiring resistances that are artifacts of the layout. In addition, the sensitivity of the design to scaling must be examined, so the circuit may be modified as necessary to compensate for scaleability.

Neural Network Components

To generate the more common elements employed in neural networks, two simple circuit blocks are required, first an adder or summer with controllable weights, and second a sigmoidal transfer function similar to a digital comparator without hysteresis. Mead has shown examples of both circuits, employing the common OTA element again. Simplifications are possible and are being examined in ongoing work at FAU [18]. The method of attack is the examination of the neural building blocks from Mead, using the improvements of a scaleable OTA. Change of scale presents unknowns as to the performance and behavior of a network as its scale is changed. The differences to be expected in a change of scale arise from the alteration of transconductance of the devices and the OTA, the necessary scaling of parasitic wiring capacitances and resistances.

V. SUMMARY

We have evolved a low power dissipation high density analog cell library useful for artificial neural network applications. Attempts are underway to make the library scaleable.

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VIII. FIGURE LEGENDS

Fig. 1 Simple N-Channel Wilson Current Mirror

Fig. 2 Improved N-Channel Wilson Current Mirror

Fig. 3 Improved P-Channel Wilson Current Mirror

Fig. 4 Improved Widlar N-Channel Current Mirror

Fig. 5 Improved Widlar P-Channel Current Mirror

Fig. 6 Current Reference Cell: Circuit Schematic

Fig. 7 Current Reference Cell: (a) HSPICE Simulation and (b) Test Results

Fig. 8 Simple OTA: Circuit Schematic

Fig. 9 Simple OTA: Small Signal Behavior. (a) HSPICE Simulation and (b) Test Results

Fig. 10 Simple OTA: Large Signal Behavior Test Results

Fig. 11 Wide Range OTA: Circuit Schematic

Fig. 12 Wide Range OTA: Small Signal Behavior. (a) HSPICE Simulation and (b) Test Results

Fig. 13 Wide Range OTA: Large Signal Behavior. (a) HSPICE Simulation and (b) Test Results

Fig. 14 Follower Integrator: Circuit Schematic

Fig. 15 Follower Integrator: (a) HSPICE Simulation and (b) Test Results

Fig. 16 Second Order Low Pass Filter Section

Fig. 17 Gilbert Multiplier: Circuit Schematic

Fig. 18 Gilber Multiplier: (a) HSPICE Simulation and (b) Test Results

Fig. 19 MOSFET I vs V Characteristic

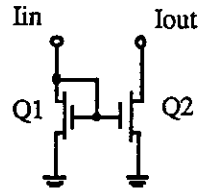


Figure 1

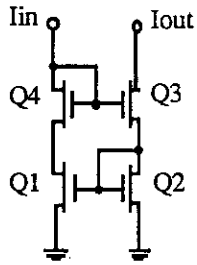


Figure 2

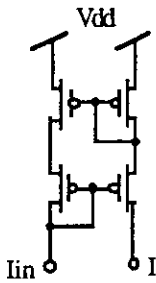


Figure 3

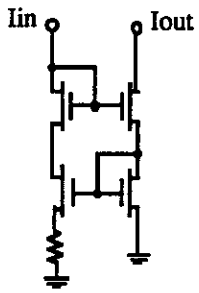


Fig. 4

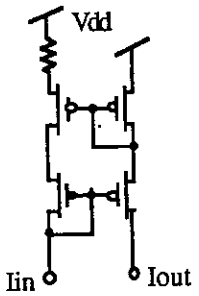


Fig. 5

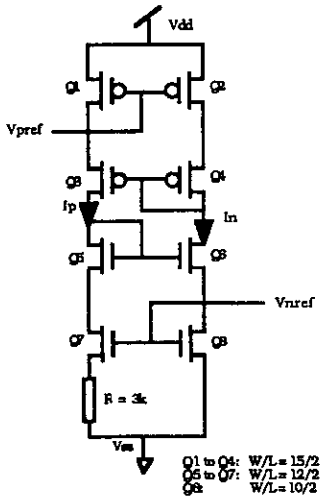


Fig. 6

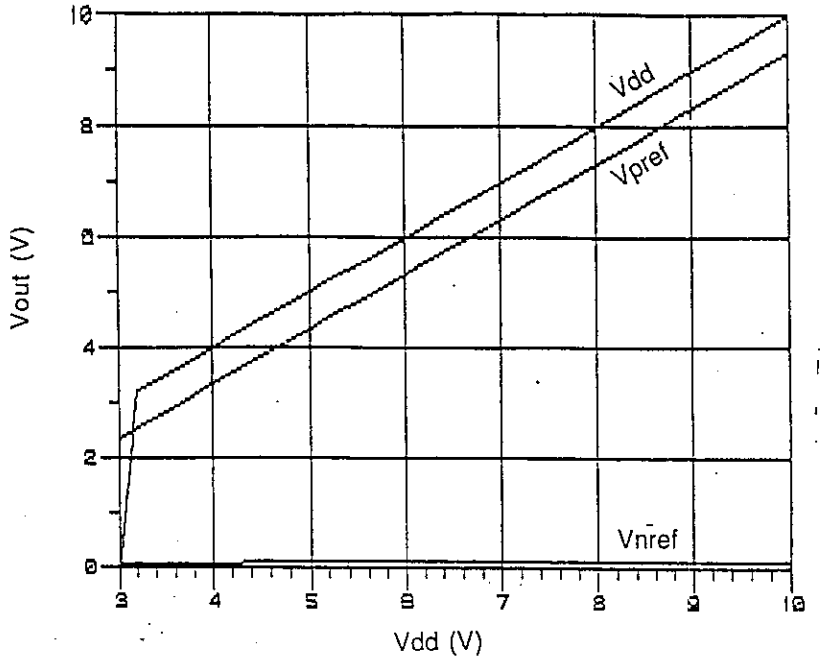


Figure 7 (a)

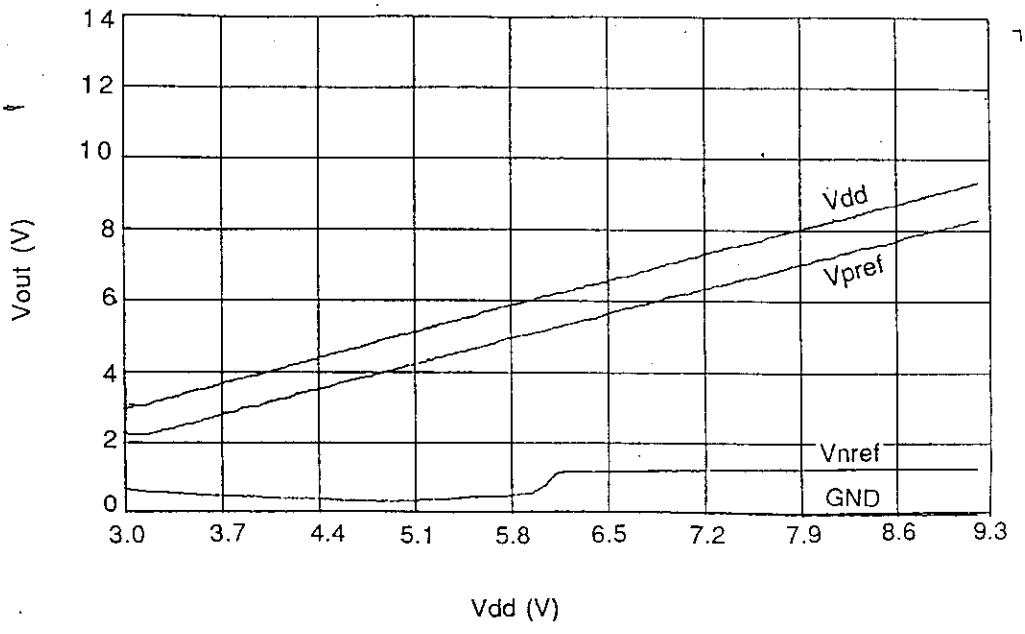


Figure 7 (b)

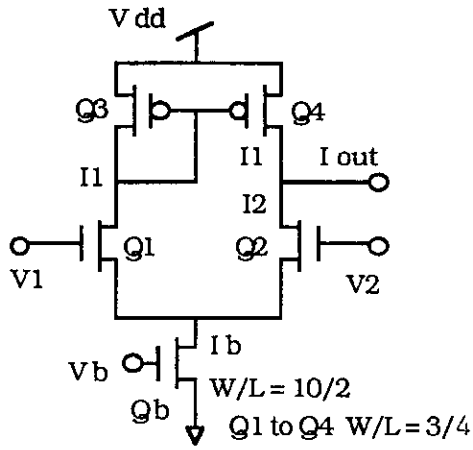


Figure 8

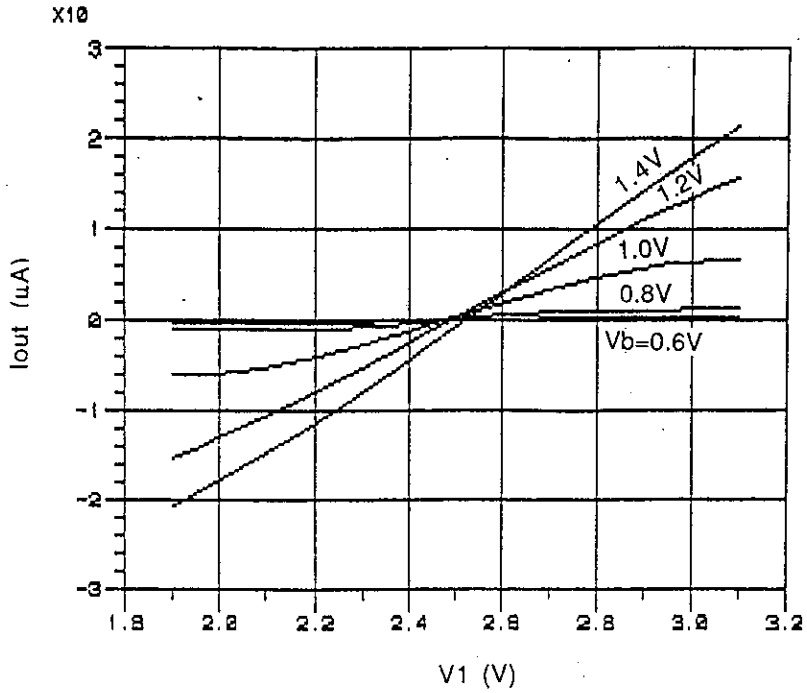


Figure 9 (a)

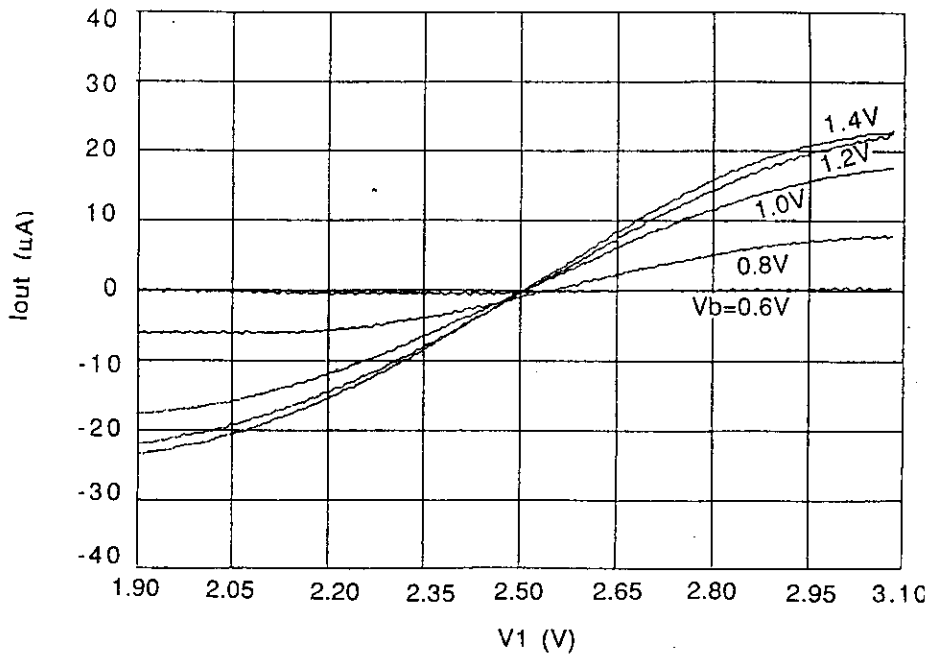


Figure 9 (b)

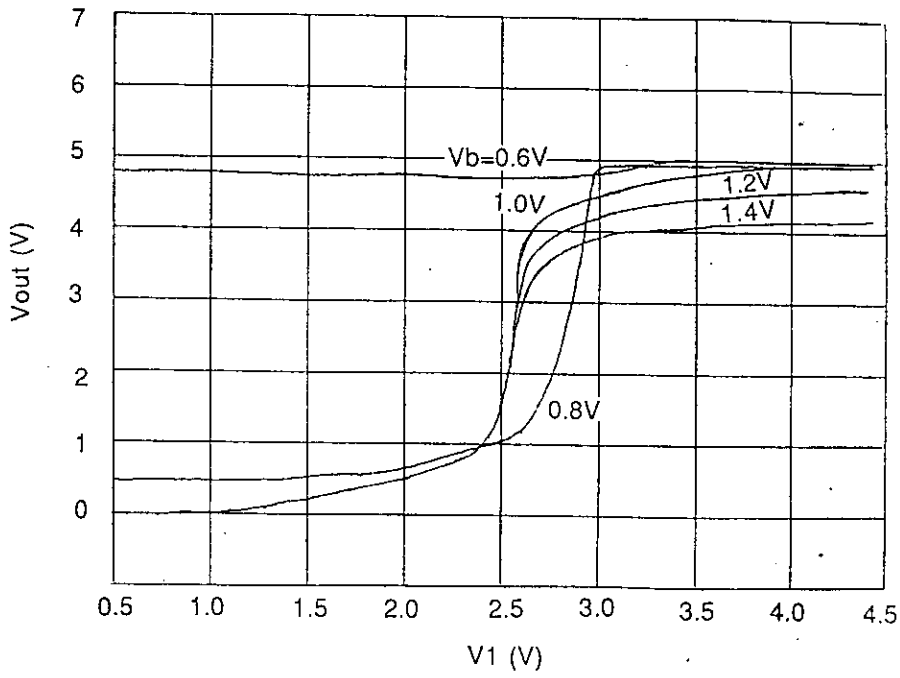
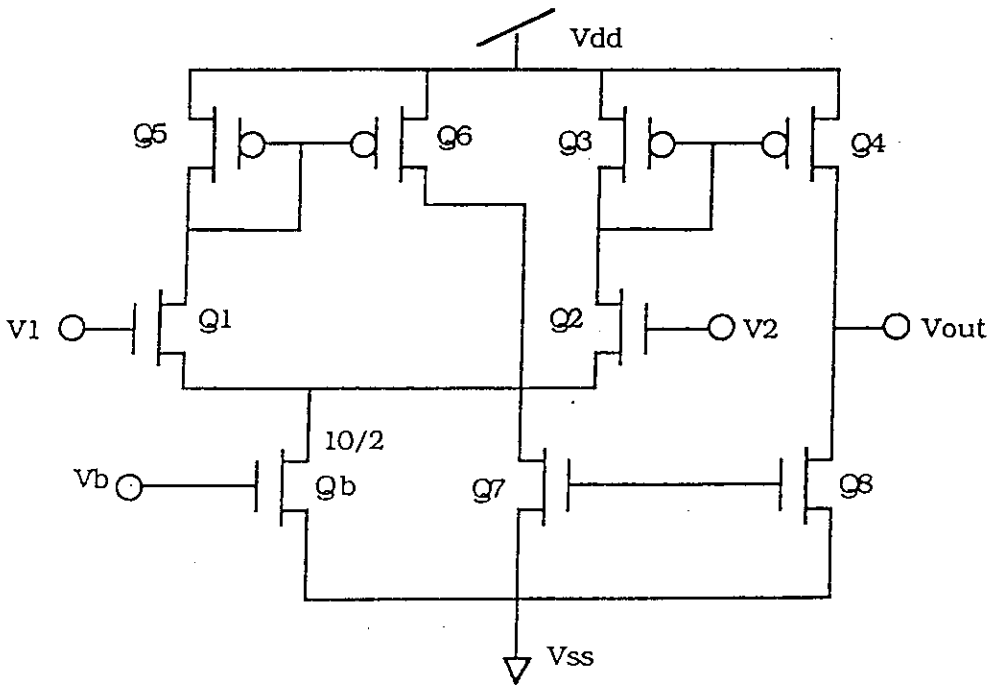

7
6
5
4
3
2
1
0
Vout (V)
Vb=0.6V
1.0V
1.2V
1.4V
0.8V
0.5
1.0
1.5
2.0
2.5
3.0
3.5
4.0
4.5
V1 (V)

Figure 10



Q1 to Q8: W/L = 3/4

Figure 11

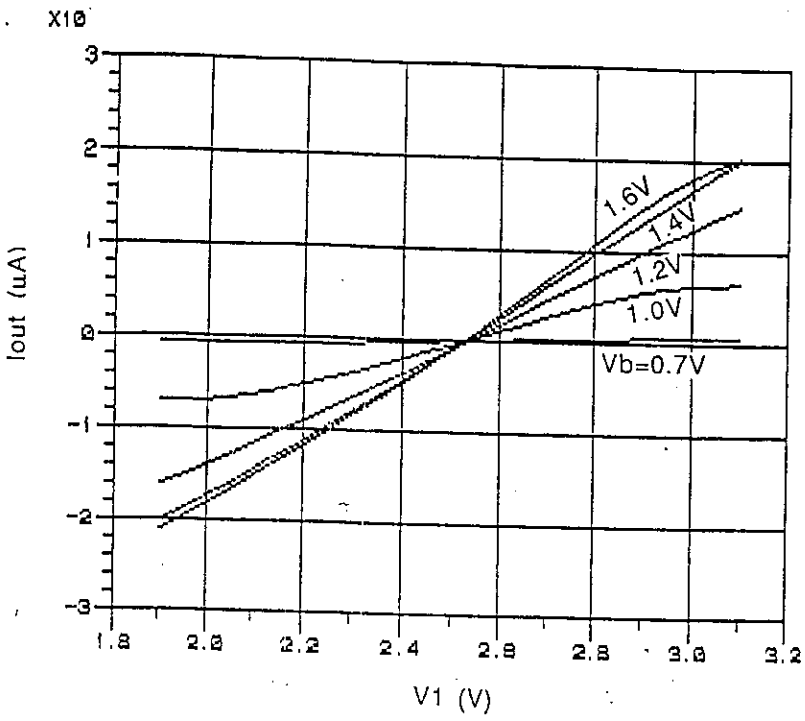


Fig. 12(a)

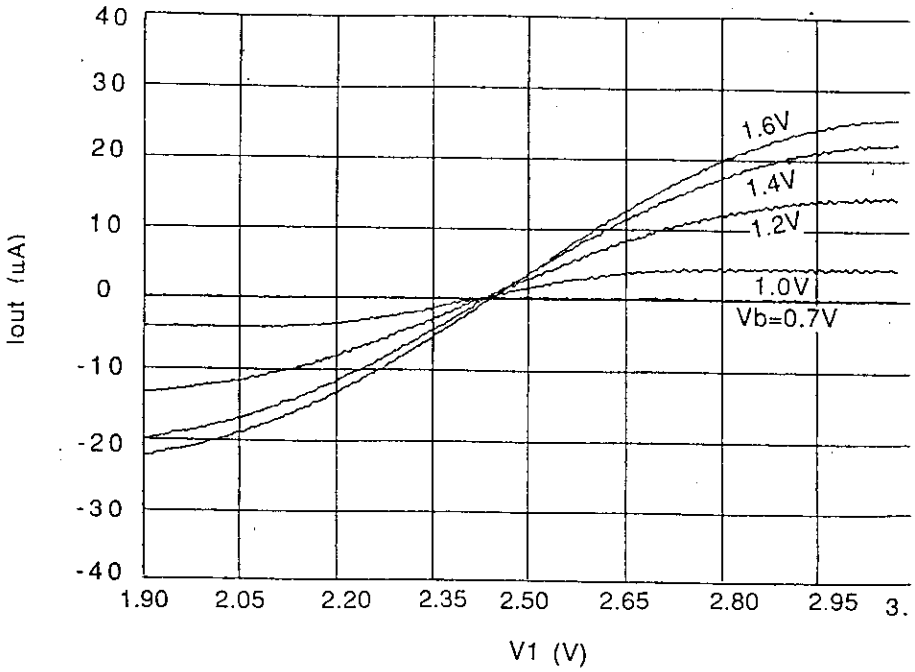


Fig. 12(b)

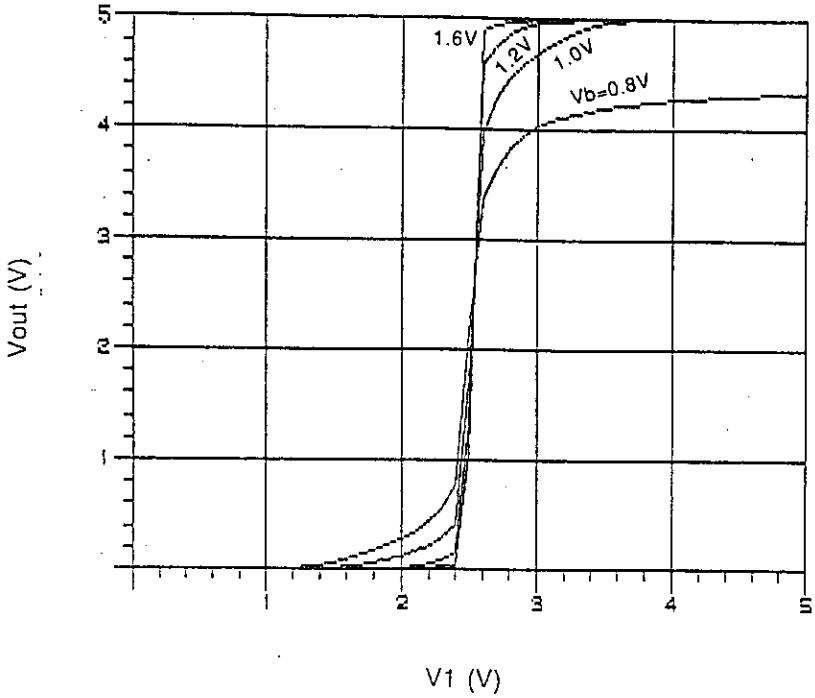


Fig. 13(a)

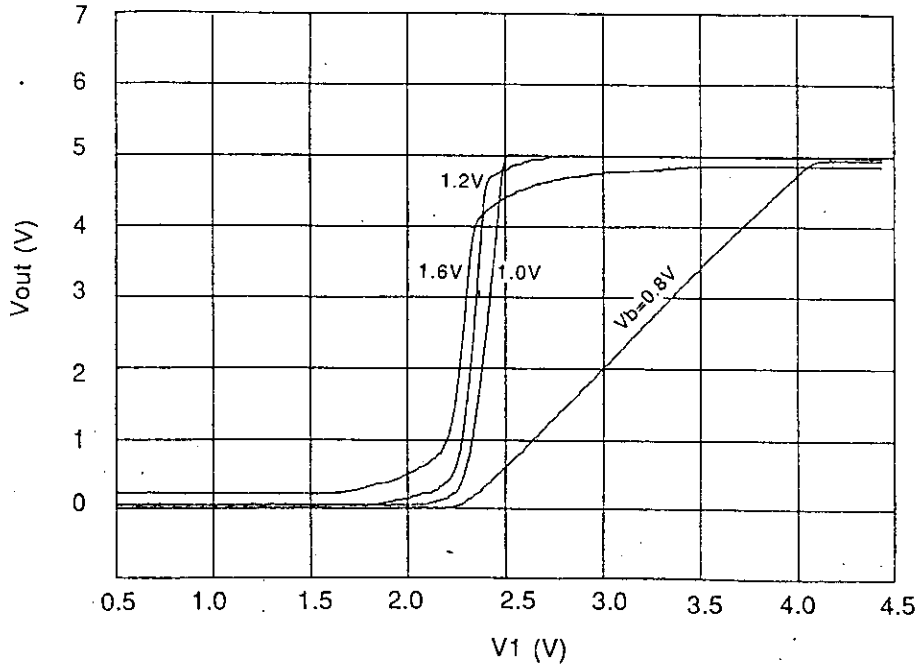
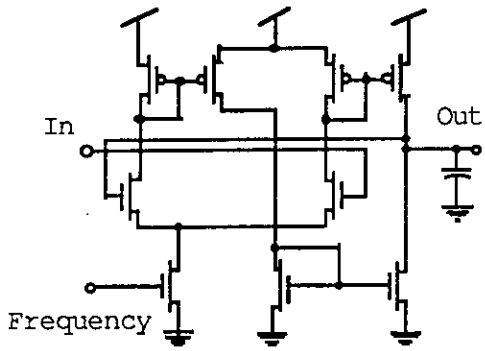


Fig. 13(b)



Follower-integrator Schematic

Figure 14

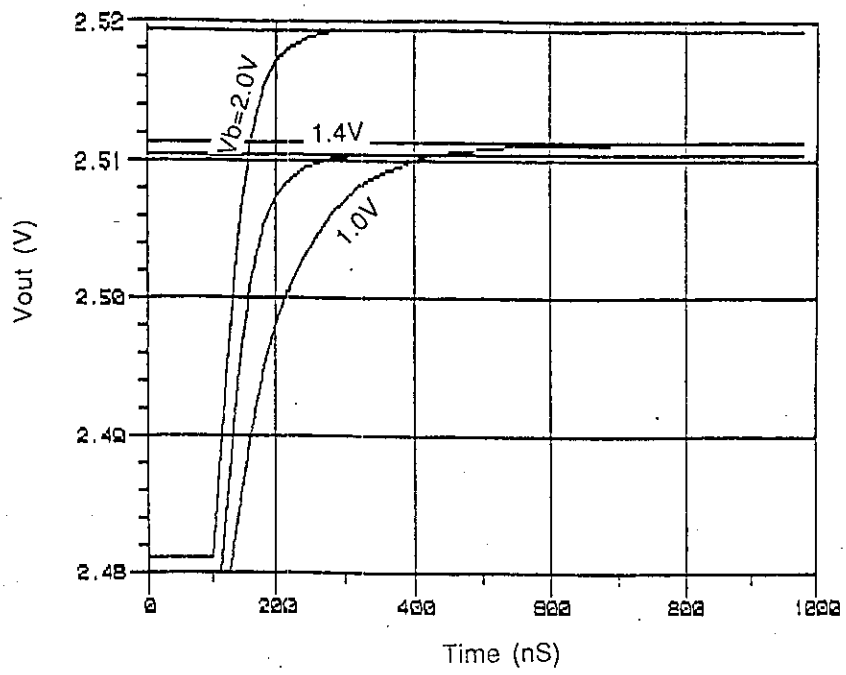


Figure 15 (a)

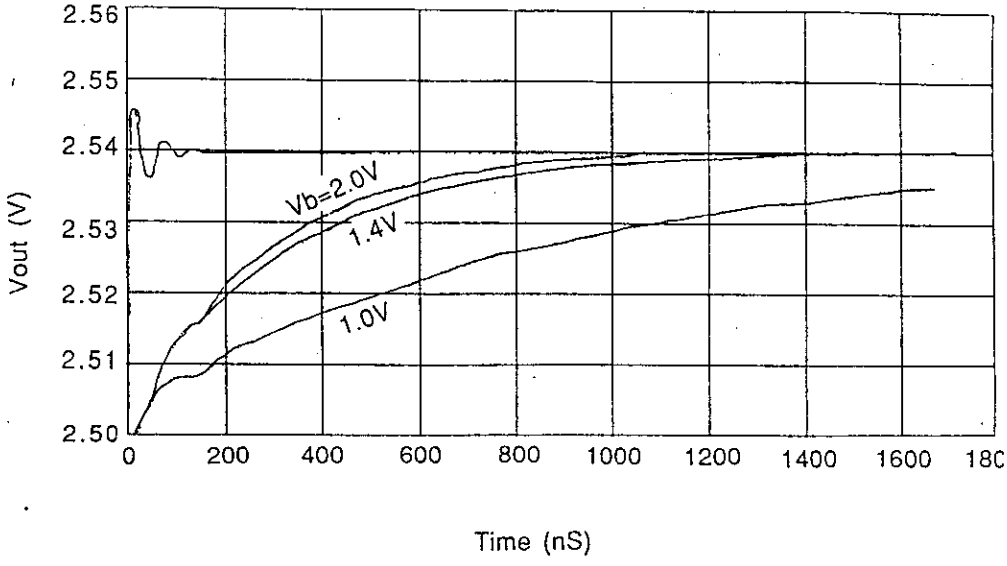
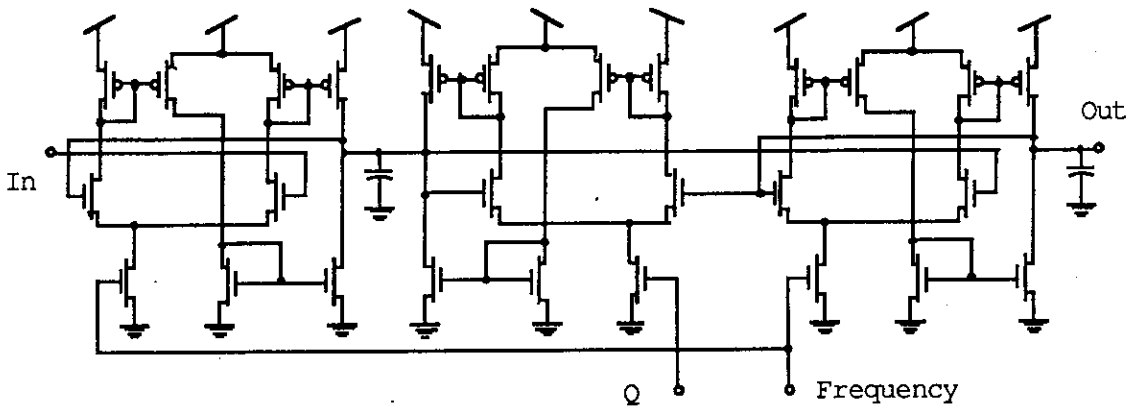


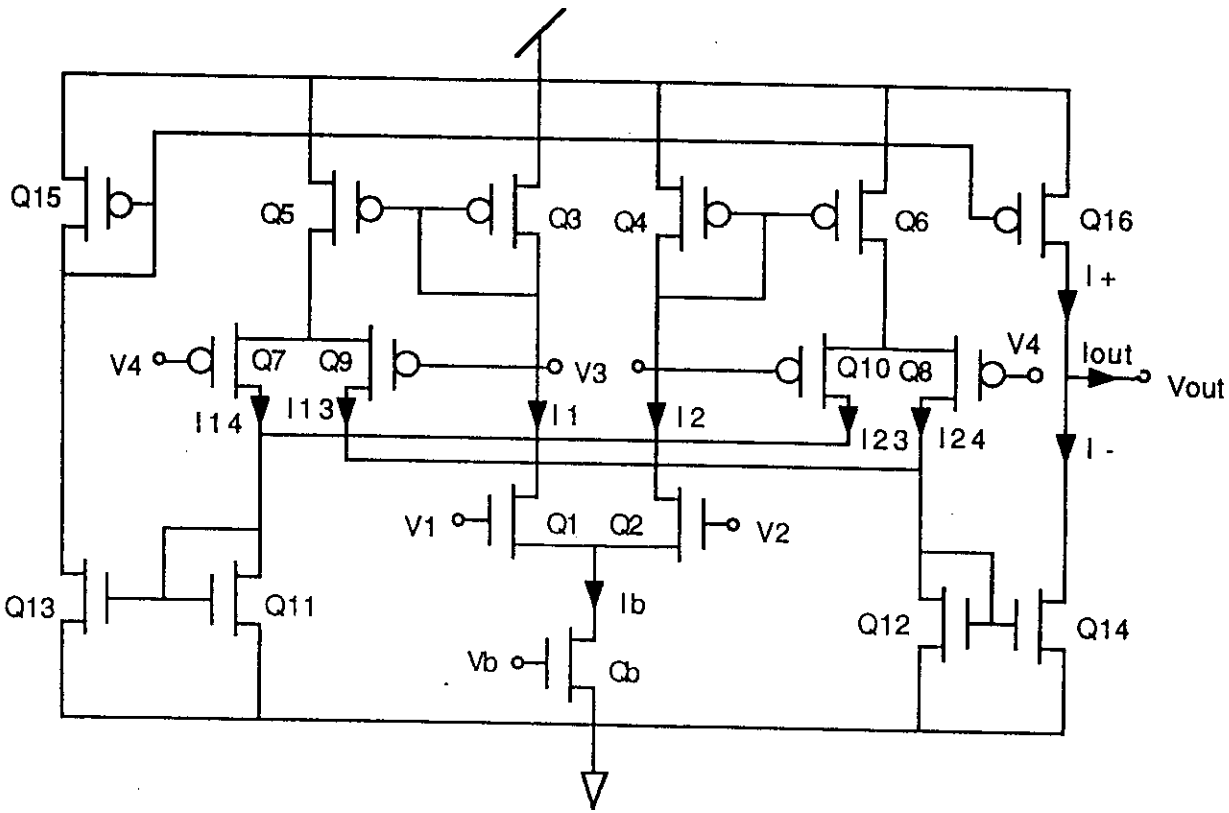
Figure 15 (b)



Second Order Lowpass Filter Section

Figure 16

Gilbert Multiplier



Q1, Q2, Q11, Q13:	W/L = 12/2	Q12, Q15:	W/L = 4/4
Q3, Q4, Q5, Q6:	W/L = 10/2	Q14, Q16:	W/L = 3/40
Q7, Q8, Q9, Q10:	W/L = 13/2	Qb:	W/L = 3/22

circuit diagram

Figure 17

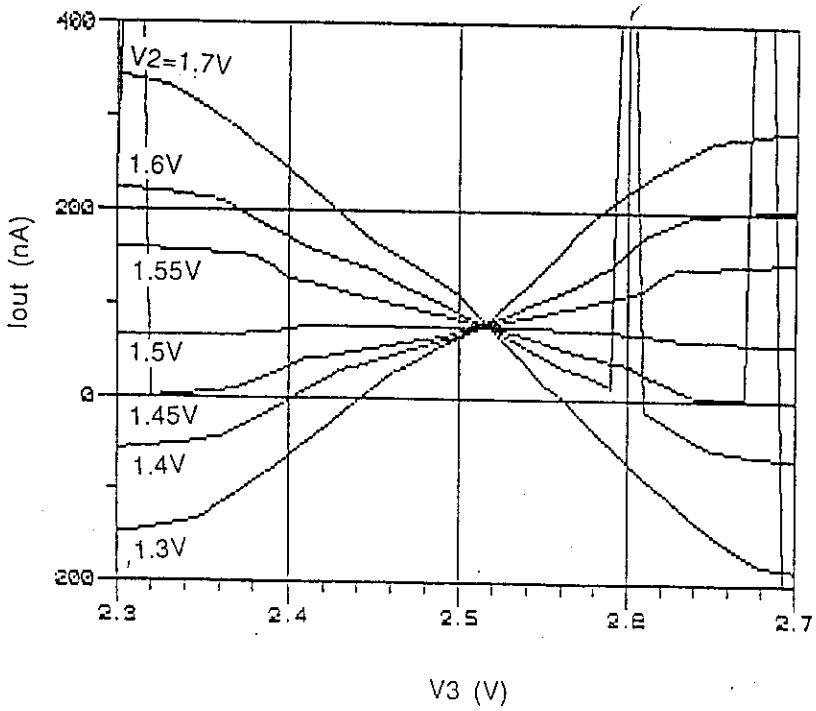


Figure 18 (a)

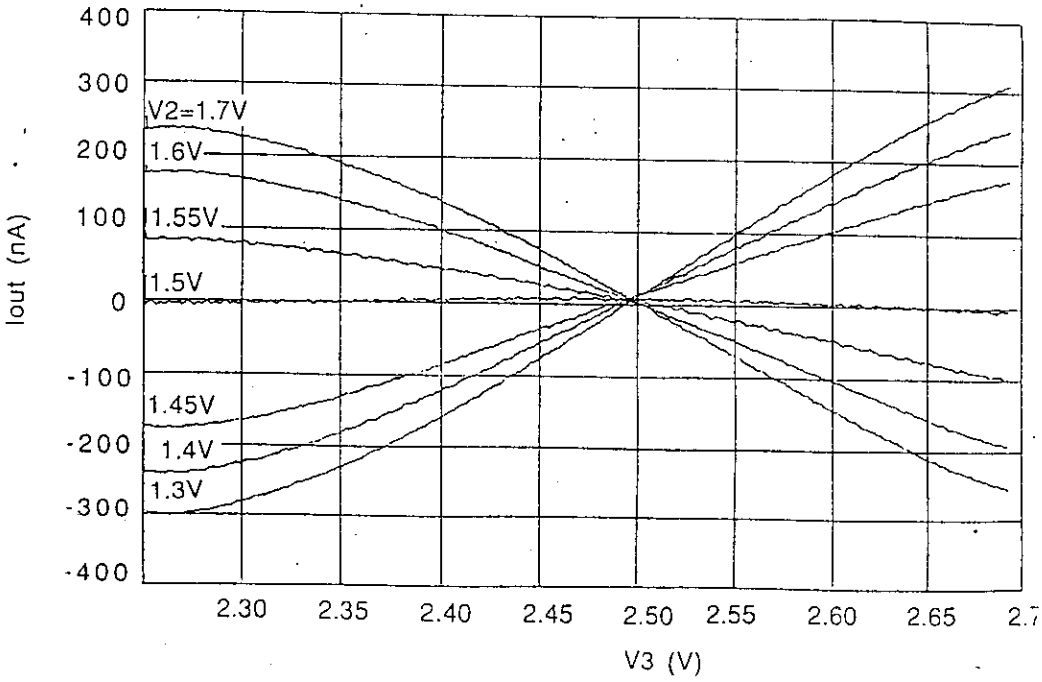


Figure 18 (b)

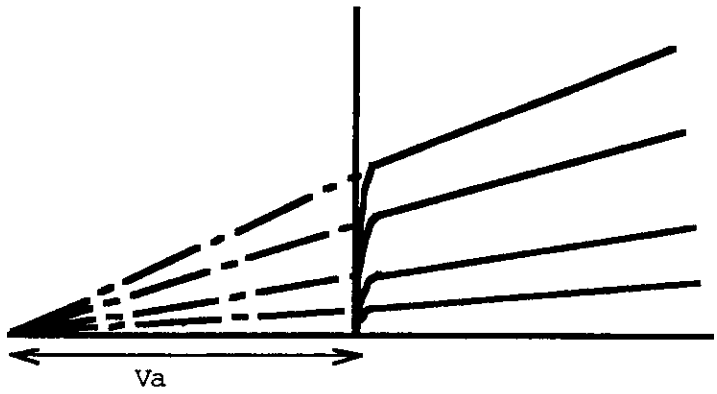


Figure 19 MOSFET v versus i characteristic