Efficient Mapping Of A Handwritten Digit Recognition System Onto Intel's ETANN Chips.

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Abstract This paper describes mapping of a twenty one CLUMP module network onto three Intel's ETANN (80170NW) chips. ETANN is a sixty four neuron general purpose neural network chip. The chip essentially has sixty four single layer neurons, with enough flexibility to use in different configurations. We use the chips in a time multiplexed mode to enhance utilization of chips. To avoid conflicts in using various resources, a program was written to show the usage of inputs, neurons, and weights. By studying the results of the program it was possible to bring down the number of chips from nine in the initial draft to three chips in the final design.

Introduction The simulated neural network used for handwritten digit recognition consists of twenty one CLUMP (clustered multi layer perceptron) modules [1]. Each module comprises of three layers, with 10, 8, and 1 neurons in the input, the hidden, and the ouput layers respectively. Figure 1(a) shows the architecture of the CLUMP module. Each module has thiry two inputs and all modules are fed with the same input data. Figure 1(b) shows the network configuration with twenty one CLUMP modules. Intel's ETANN (80170NW) is essentially a single layer sixty four neuron network with a flexible architecture. Flexible architecture facilitates it to be used as a two layer network, or as a128 input network, etc. Details of some configuration are given in [2].

Methodology In order to map the twenty one CLUMP module network onto ETANNs and to keep the chip count to a minimum, time multiplexing was adopted. Concepts utilized are stated below:

1. Repeated use of neurons is possible by feeding select inputs to the network during each clock phase. For example, in ETANN chip#1 neurons 1 to 60 are used with inputs 1 to 32 active during phase 1. While during phase 4, inputs 33 to 64 are active and same neurons 1 to 60 are used.

2. Different sets of inputs can be fed on the same input lines during different phases, such multiplexed usage of inputs is possible, since only selected outputs are considered.

Based on the above mentioned techniques, a twenty one module network was mapped onto a circuit consisting of three 80170NW chips.

Operation A total of twelve phases are required to obtain the desired twenty one outputs. Figure 2 shows utilization of chips during different phases. Hardware details for operation are not shown in fig. 2. During phase one, chip 1 implements the first layer of six CLUMP modules. During phase two, chip 2 operates in feed forward mode. It receives input from six input layers, resulting in forty eight outputs. During phase three, chip 3 in the feedback mode (external inputs) gives the final six outputs. During following phases similar operations take place with variation of inputs and modes of chip operation.

Results The total number of neurons in the CLUMP architecture is 399 (19*21), and the number of weights is 8568 (408*21). A network of three ETANN chips consist of 192 (64*3) neurons and 24,576 (8192*3) weights. Thus effective mapping of several small networks onto a general purpose large network is possible.

Conclusion Very effective utilization of neurons was acheived. Mapping of a large number of small networks resulted in marginal utilization of weights. However further explorations may result in better utilization of all the weights available.

References

- [1] Lawerence Agba., Ph.D Thesis, Florida Atlantic University, Boca Raton Fl.
- [2] 80170NW techinical information manual (experimental), from Intel Corporation, 1990.

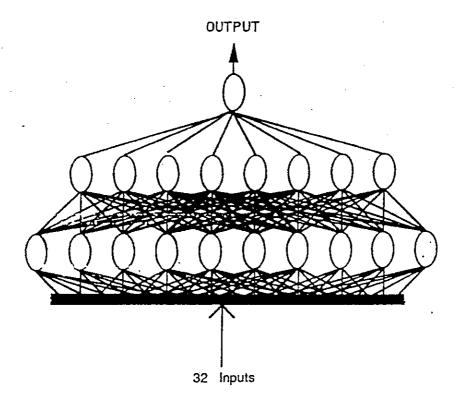


Figure 1(a) CLUMP Module Architecture

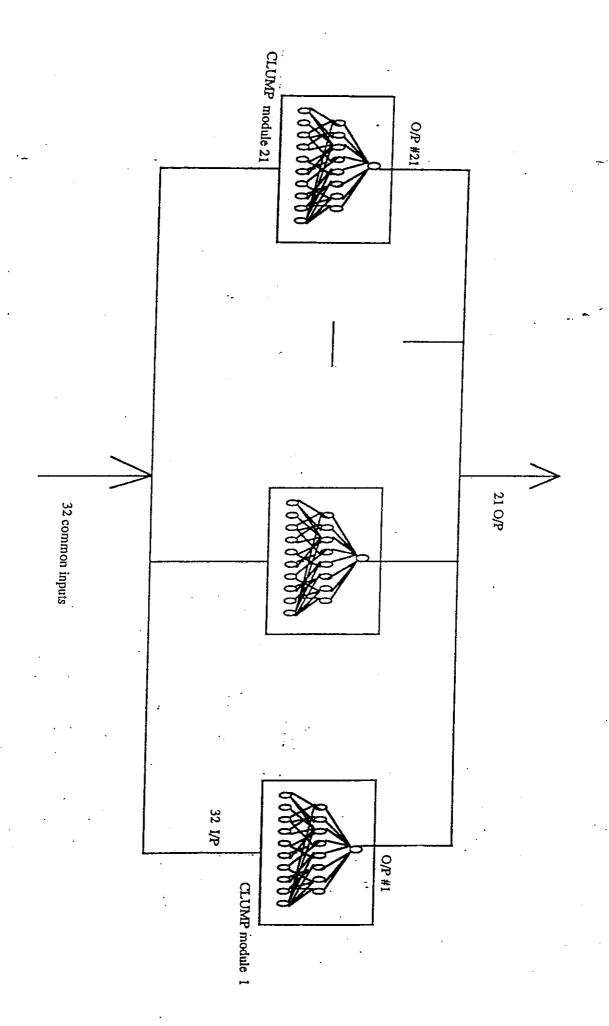


Figure (1b) CLUMP Network used for handwritten digit recognition system.

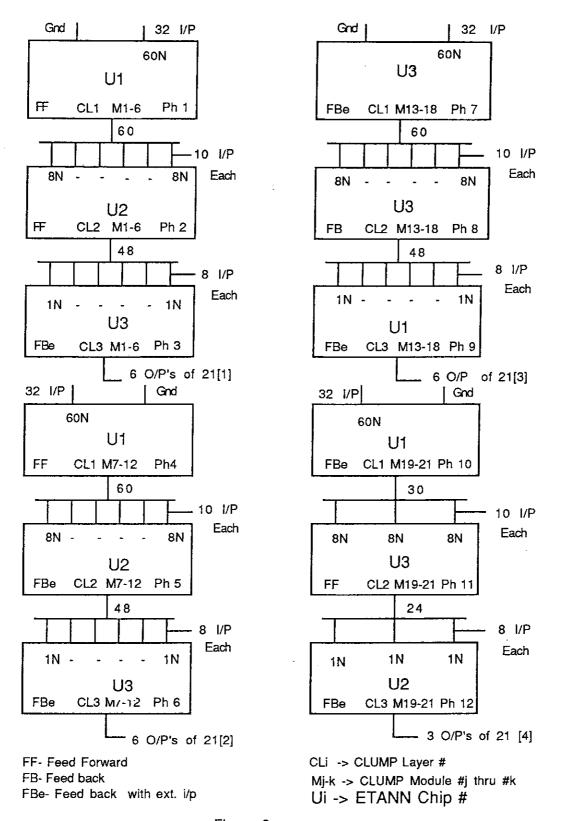


Figure 2

CHIP 1

EVALUATING USACE OF ETANN CHIP FEED FORWARD WEIGHT MAIRIX

Neurons>		
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n		
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	42 43	
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	58	44444444444444444444444444444444444444
- 4	59 50	<u></u>
- }	i ra	<u> </u>
	57 i	<u> </u>
-	53 [44444444444444444444444444444444444444

PERCENTACE USAGE OF WEIGHTS IN FEED FORWARD MODE => 93,750000

U - Unused

1 thru C - Clock Phases (Hex notation)

FEED BACK WEIGHT MATRIX

```
Neurons --->
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   Pu
   I SOCCOORDANGEMENTE TO THE TRANSPORT OF 
   16
   17
   18
 19
   20
   28
  37
  \odot
38
  40
  \odot
  53
 \mathsf{j}
 10000000
```

PERCENTAGE USAGE OF WEIGHTS IN FEEDBACK MODE =>32.746822

TOTAL PERCENTAGE USAGE => 63.281250

U - Unused

1 thru C - Clock Phases (Hex notation)

EVALUATING USAGE OF ETANN CHIP FEED FORWARD WEIGHT MATRIX

```
Neurons --->
n
11
15
22
23
24
25
26
27
30
31
32
33
37
48
49
50
51
52
53
54
55
56
57
58
59
60
61
```

PERCENTAGE USAGE OF WEIGHTS IN FEED FORWARD MODE => 79.687500

U - Unused

- 1 thru C Clock Phases (Hex notation)
- 0 Weights set to zero because smaller networks are mapped onto a larger network and inputs are given at the same instant. Hence to nullify the other layer inputs weights are initialized to zero.

FEED BACK WEIGHT MATRIX

```
P
5
53
54
55
56
57
```

PERCENTACE USAGE OF WEIGHTS IN FEEDBACK MODE =>74.975563

TOTAL PERCENTAGE USAGE => 77.343750

U - Unused

1 thru C - Clock Phases (Hex notation)

EVALUATING USAGE OF ETANN CHIP

FEED FORWARD WRIGHT MATRIX

```
Neurons --->
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n
  31
      32
      47
      51
52
53
54
55
56
57
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```

PERCENTAGE USAGE OF WEIGHTS IN FEED FORWARD MODE $\Longrightarrow 70.312500$

U - Unused

1 thru C - Clock Phases (Hex notation)

FEED BACK WEIGHT MATRIX

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Neurons --->
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   1
   2
put
 3
   4
5
   6
7
8
   28
  29
  30
31
  33
  34
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  36
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  38
39
  40
  | OCCOSSO OCCO
42
43
  46
47
48
  49
50
51
52
53
54
55
56
57
  61
```

PERCENTAGE USAGE OF WEIGHTS IN FEEDBACK MODE => 92.179863

TOTAL PERCENTACE USACE => 81,250000

U - Unused

1 thru C - Clock Phases (Hex notation)